TCAD-based performance analysis of nanoscale vacuum field-emission transistors at advanced technology nodes

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At the present time, the significant progress has been made in the area of scaling of solid-state nanoelectronic devices, where minimal design standards approach a level of 10 nm and below [1]. With the decrease in the lithographic dimensions of MOS transistors, the influence of interface effects near the border with the conductive channel region becomes critical. In particular, the complexity of technological control of the gate oxide thickness and the occurrence of additional leakage current can lead to rapid degradation of operating characteristics in harsh environment. Simultaneously, electron-phonon scattering in a semiconductor material initially limits performance of MOS transistor. Field emission of electrons into the vacuum provides maximum charge-carrier lifetime and high frequency (in the THz range)/power ratio, which makes field-emission transistors with nanoscale vacuum channel the most attractive for the high-speed electronic devices which operate under the high radiation and temperature conditions. However, low stability of current emission and strong power consumption in the modern vacuum microelectronic devices demands improvements in the fabrication process of the vacuum transistors.

Recent development of vacuum transistor with nanoscale air channel [2] opens the way to the creation of a new class of vacuum nanoelectronic devices in which electrons move in a "quasi-vacuum" with a minimum probability of collision with gas molecules at a channel length of less than 100 nm. This approach significantly reduces the power consumption of vacuum nano-transistors and prevents the degradation of emission characteristics. In addition, increasing emission current from a single cathode requires a reduction of the emitter radius up to the nanometers. Technological computer-aided device (TCAD) simulation becomes an important tool for the reducing the cost of producing the test structures of vacuum transistors.

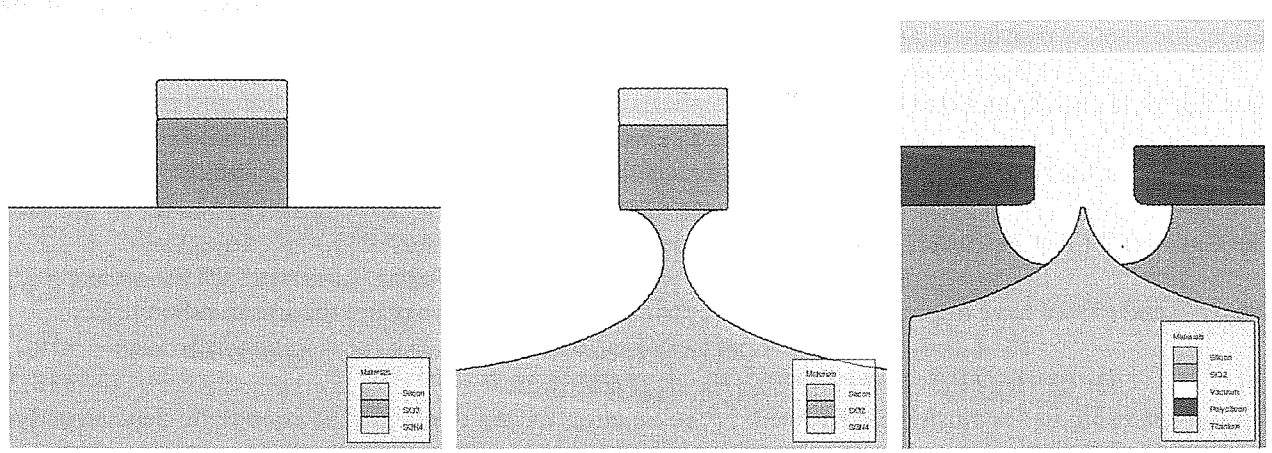

Figure 1. Technological steps of the fabrication process of nanoscale vacuum transistor.

In this work the full fabrication process of both gate-all-around nanowire and nanoscale vacuum channel transistors (Fig. 1) has been simulated using Silvaco TCAD (Victory Process and Victory Device simulation modules [3]). The analysis of electric characteristics of the obtained structure of vacuum transistor shows the comparability of the operating currents with an improved performance compared to its solid-state analog for different technology nodes varied from 50 to 5 nm. The obtained parameters of fabrication process can serve as recommendations for the development of a new generation of high-speed nanoscale vacuum transistors.

1. R. Courtland. "Moore's Law's Next Step: 10 Nanometers". IEEE Spectrum, **54**, pp. 52-53, 2017.
2. J.W. Han, D.I. Moon, and M. Meyyappan. "Nanoscale Vacuum Channel Transistor". Nano Lett., 17 (4), pp. 2146–2151, 2017.
3. Silvaco TCAD tools: Victory Process User's manual, Process Simulation Software, 2018.