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TCAD-based performance analysis of nanoscale vacuum field-emission transistors at advanced technology nodes

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ABSTRACT

Full fabrication process of nanoscale vacuum channel and gate-all-around nanowire transistors at the 45, 32 and 22 nm technology nodes was simulated in Silvaco TCAD. Comparative analysis of operation modes was made on the basis of the obtained structures. It was shown that nanoscale gate-all-around transistor has sufficiently low power consumption while vacuum channel field effect transistor makes it possible to achieve performance that exceeds performance which can be obtained from the transistor with semiconductor channel. The combination of the above technologies can serve as approach to the creation of low-power and high-speed nanoscale vacuum devices using established complementary metal-oxide-semiconductor (CMOS) technology.

Keywords: TCAD, CMOS, nanoscale vacuum channel transistor, gate-all-around nanowire transistor, technology node

1. INTRODUCTION

Today significant progress has been achieved in the area of scaling of nanoelectronic devices, where minimal design standards approach a level of 10 nm or even below[1]. However, at the same time, it becomes clear that design standards of nanoelectronics have almost reached its physical limits. A further development in the field of miniaturization of nanoelectronic devices requires new actual approaches and solutions. One of these approaches is a creation of transistor with non-planar geometric structure. Gate-all-around nanowire field effect transistor (GAA FET) is a great example of such new configuration. This type of field-effect transistor is a result of further improvements in construction of FinFET. Generally, GAA FET has several advantages: immunity to the short-channel effect; lower switching energy and signal propagation delay compared to FinFETs and compatibility to current CMOS technology[2,3].

It is well known that electron-phonon scattering in semiconductors initially limits performance of CMOS transistors. Replacing silicon with vacuum as a conveying medium can help to avoid performance restriction[4]. The use of nanoscale vacuum channel provides maximum charge-carrier lifetime and high frequency/power consumption ratio and eliminates the need for high vacuum since the probability of electron collisions with gas molecules in air is practically negligible on the scales of 100 nm and below. However, previous studies show that vacuum transistor has higher operation voltage than modern conventional solid state FETs, although it can be reduced by technological scaling. Additional advantage of nanoscale vacuum devices is a resistance to the harsh environmental conditions such as ionizing radiation and high temperature that would make these devices suitable for the aerospace applications[5-7].

Thus, this paper is organized as follows. Section 2 contains description of the supposed transistor structures used in simulation, numerical method for the calculation of emission current from non-planar curved emitters, and, besides that, the description of fabrication route of silicon field-emitter array. The results of simulation of the obtained transistor structures are presented in Section 3. Final conclusions are summarized in Section 4.

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2. MODELS AND BASIC EQUATIONS

Fabrication process of nanoscale vacuum channel transistor, which was implemented into Silvaco TCAD using Victory Process module[8], was based on actual fabrication process of silicon field emitter array. This array was made in the following way: n-type silicon wafers doped with phosphorus with (100) crystallographic orientation and 150 nm in diameter were used. Wafers were oxidized in wet O_2 (0.3 μm SiO_2 layer was obtained), Si_3N_4 layer was deposited as a masking layer (thickness of Si_3N_4 layer was 0.13 μm) after oxidation, and then photolithography was performed on wafers to form oxide-nitride caps for the following etching process. The curved profile of the pillars was made using plasma-chemical etching in a mixture of SF_6 and O_2 with anisotropy coefficient of 2.5.

Final oxidation process transforming silicon pillars into sharp tips was performed in dry O_2 ambient and after that SiO_2 layer along with nitride layer was removed from the substrate. The minimal radius of emitter tip curvature was about 3 nm. Figure 1 shows SEM images of the obtained structures.

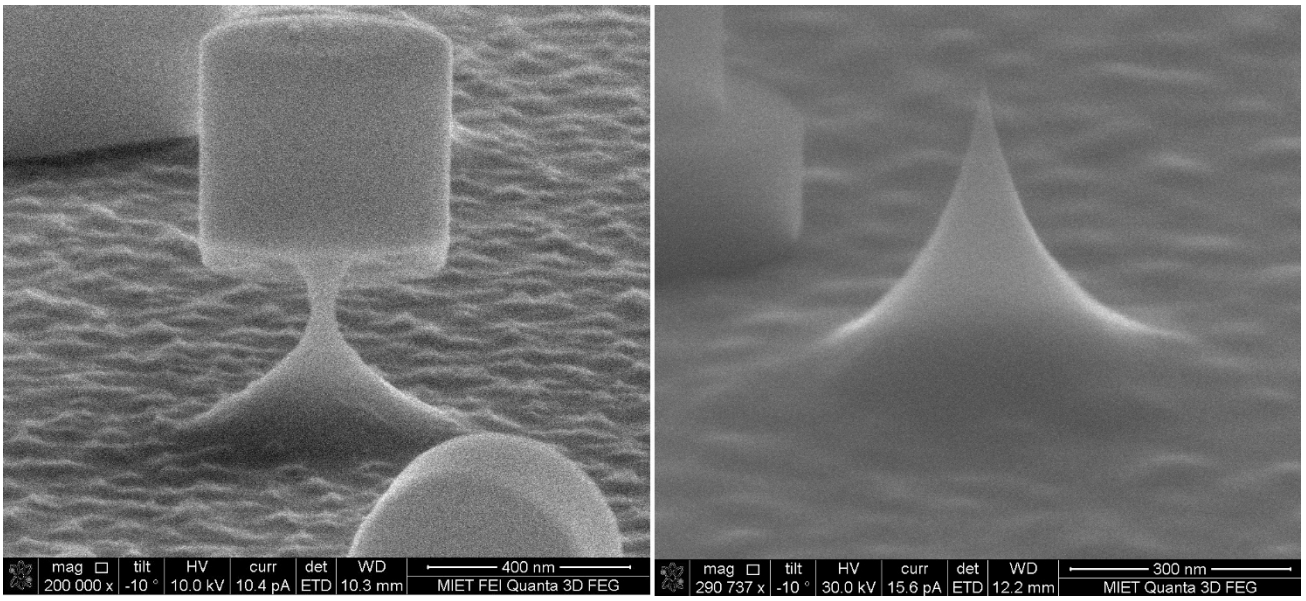

Figure 1. SEM images of the sample of field emitter array. Left: curved pillar with masking oxide-nitride cap. Right: complete silicon field emitter.

Similar fabrication process was simulated in Silvaco TCAD, but in addition to the creation of emitter tip, formation of aluminum gate (control grid) and anode electrodes was appended to the route to obtain a structure of the vertical vacuum transistor. Structural parameters of the transistor: substrate orientation – (100); substrate doping – As, 5×10^{18} cm^{-3}; radius of tip curvature – 5 nm; distance from the end of tip to gate – 25 nm. Main technological parameter of scaling was defined as a distance between anode electrode and cathode tip (according to the channel length in conventional FETs). Cathode-anode distance was varied from 45 to 22 nm. Images of transistor structure on various fabrication stages are presented in Figure 2.

The model of gate-all-around field-effect transistor was also created in Silvaco TCAD using process simulation. This model was based on the following fabrication route: lightly and highly doped N-type profiles were formed consistently on the silicon wafer with (100) orientation. Thin silicon pillars were made using etching, and oxidation of pillars was performed to obtain gate oxide. After these steps two insulating oxide and one polysilicon gate layers was deposited. Drain contacts were get from deposited aluminum layer.

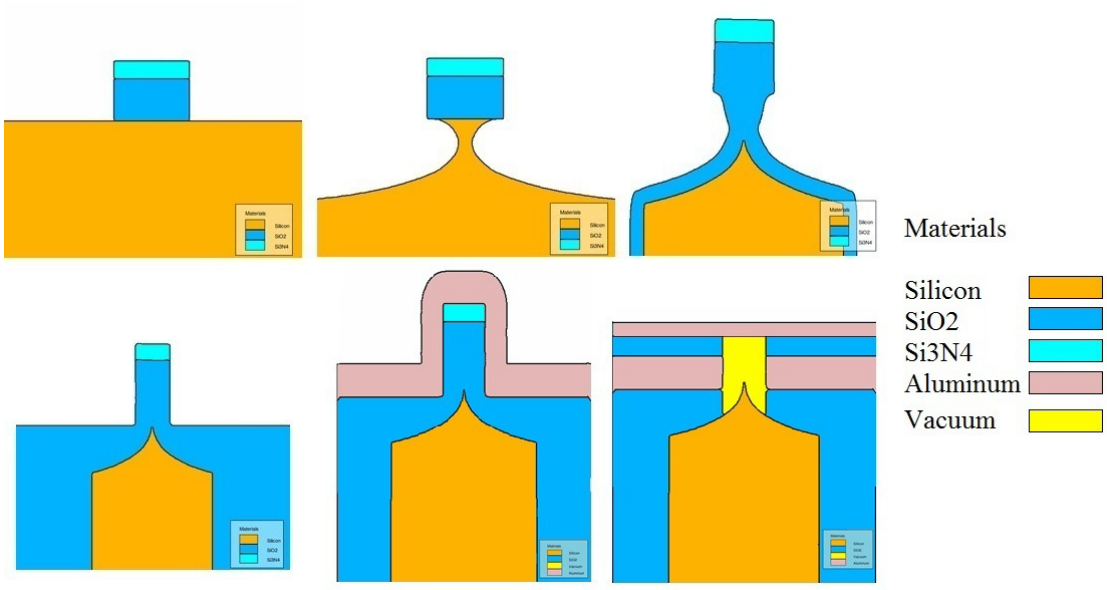

Figure 2. Images of the technological steps of formation the structure of vacuum channel transistor using Silvaco Victory Process

Structural parameters of gate-all-around nanowire transistor used in simulation: thickness of gate oxide – 2 nm; nanowire (pillar) diameter – 15 nm; nanowire length – 75 nm; source and drain doping – 1×10^{19} cm^{-3}; channel doping – 1×10^{15} cm^{-3} . Channel length was varied from 45 to 22 nm, as in the case of nanoscale vacuum channel transistor. Images of the gate-all-around transistor structure on various stages of the fabrication process are presented in Figure 3.

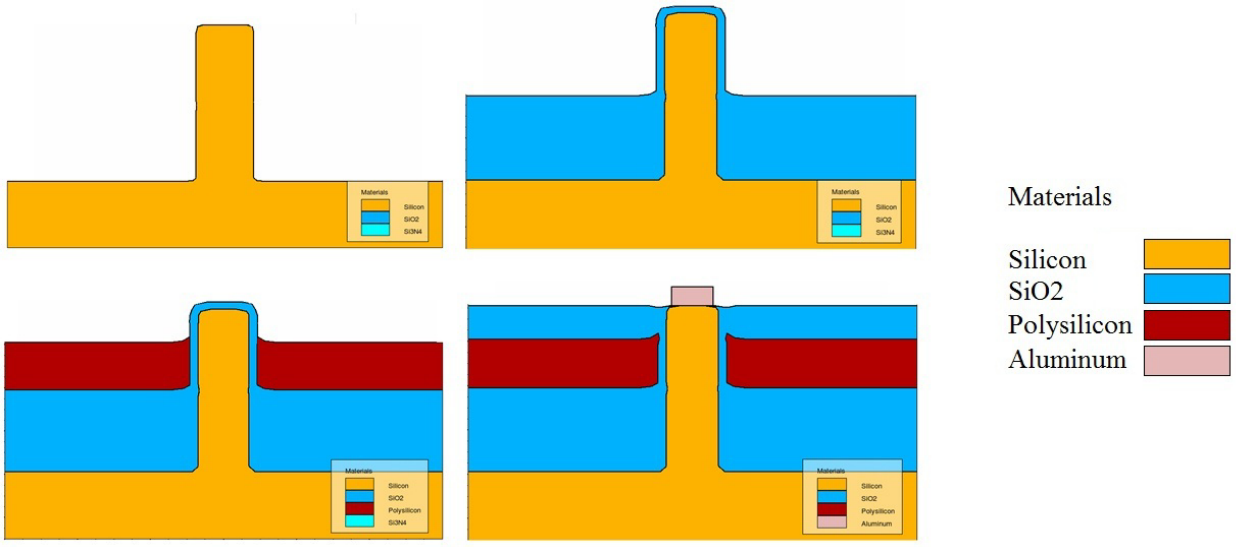

Figure 3. Images of the structures obtained during the fabrication process of nanowire gate-all-around transistor from Silvaco Victory Process.

Geometrical structure of vacuum channel transistor was imported from Silvaco TACD into COMSOL MultiPhysics[9]. Three-dimensional cylindrical model of vacuum transistor was made on the basis of transistor structure. This model is shown in Figure 4.

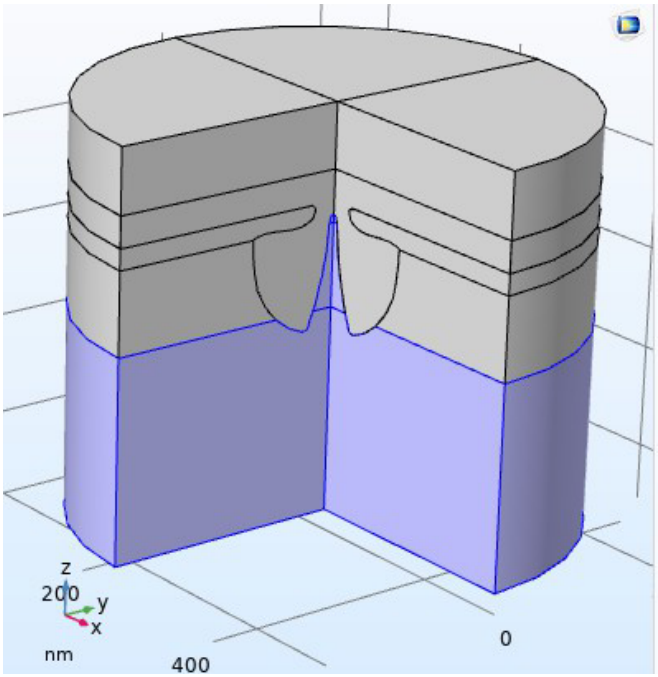

Figure 4. 3D model of vacuum channel transistor used in COMSOL MultiPhysics.

Full 3D electrostatic simulation of vacuum nano-channel transistor and electron transport from emitter to anode was performed, where the emission current from a silicon tip was calculated taking into account the geometry of the tip by performing the integral over emitting surface:

$$I = \iint_{\substack{\text{emitting} \\ \text{surface}}} JdS = JA_{\text{eff}} \quad (1)$$

Where I is resulting emission current, J is emission current density, and A_{eff} is effective area of emission.

Victory Device simulator was used to get current voltage characteristics of the gate-all-around field-effect transistor. Model of Shockley-Read-Hall recombination using concentration dependent lifetimes (SRH) and transverse-electric-field dependent mobility model (CVT) were used during device simulation[11].

3. RESULTS

Figure 5 presents the current-voltage characteristics of the vacuum channel transistor with variation of the cathode anode distance. Figure 6 shows the current voltage characteristics of emission current recalculated in the Fowler-Nordheim coordinates. Voltage at anode electrode was fixed at 90 V. It can be seen, that emission occurs at a gate voltage of about 25 V.

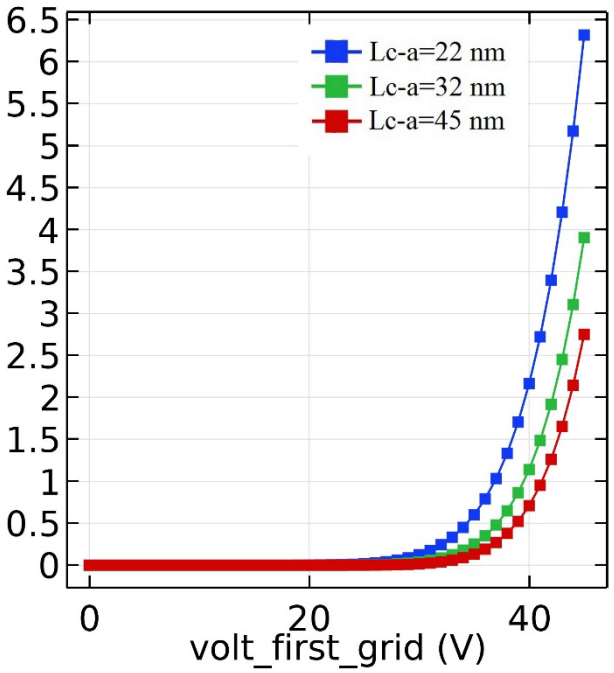

Figure 5. Current voltage characteristics of the vacuum channel transistor at different cathode-anode distances.

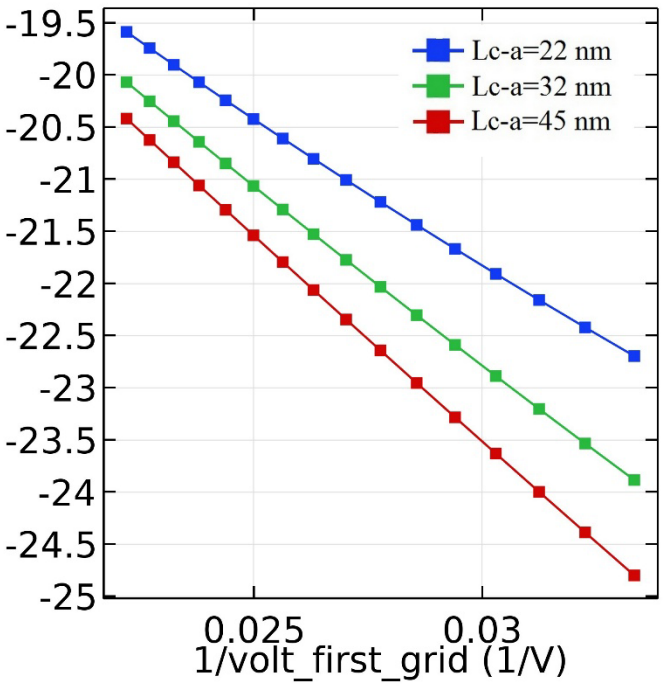

Figure 6. Current -voltage characteristics of the vacuum channel transistor at different cathode-anode distances (in the Fowler-Nordheim coordinates).

Figure 7 shows electric field distribution on the surface of emitter tip measured in V/nm. It is clearly seen that electrical field distribution agrees well with the theoretical model. Analysis of the distribution as a function of the cathode-anode distance also showed that when the distance decreases, the influence of the transistor gate increased, which can interfere

with the normal functioning of the device. Cut-off frequency dependence of the transistor that defines its performance was also derived from calculating the time spending for recharging of the cathode-gate capacitance. This characteristic is shown at Figure 8.

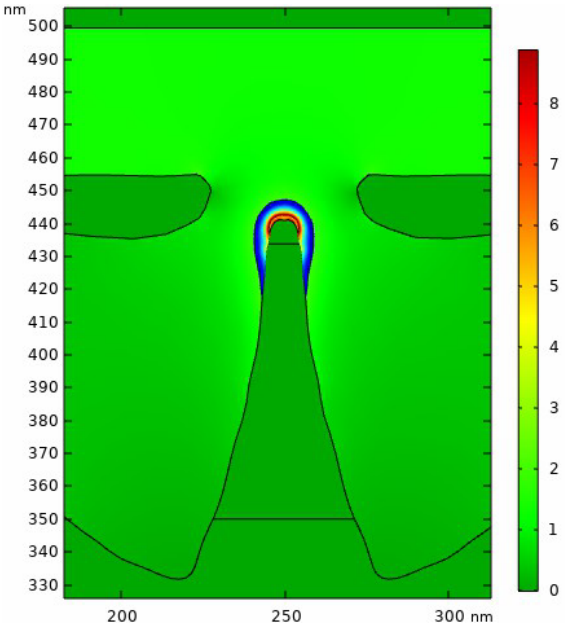

Figure 7. Electric field distribution on the emitting cathode surface.

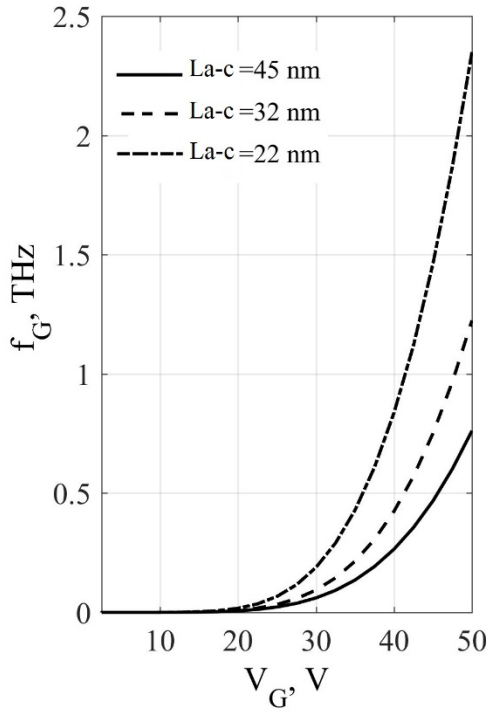

Figure 8. Curve of the cut-off frequency of the transistor depending on the gate voltage with varied cathode-anode distance.

Current voltage characteristics of the gate-all-around nanowire transistor are shown in Figure 9. Voltage at drain electrode was fixed at 0.65 V. Gate-all-around transistor exhibits high drain current in the scale of 10^{-3} A at relatively low drain and gate voltages.

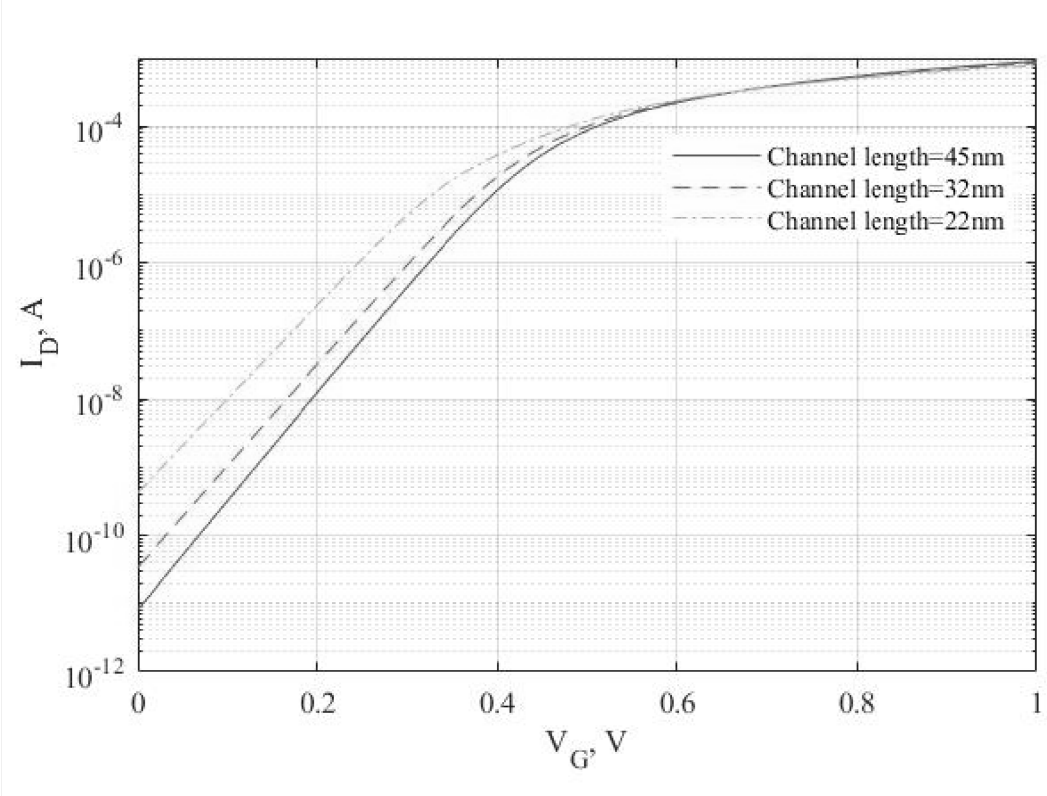

Figure 9. Current voltage characteristics of the nanowire gate-all-around transistor at different channel lengths.

4. SUMMARY

Fabrication processes of nanoscale vacuum channel transistors and gate-all-around nanowire transistors at the 45, 32 and 22 nm technology nodes were simulated in Silvaco TCAD. Three-dimensional model of the vacuum channel transistors for finite element simulation of emission current was created in COMSOL MultiPhysics simulation software. Obtained current voltage characteristics of the vacuum channel transistors showed that emission current occurs at the relatively high operating voltages, which can cause energy consumption problems. At the same time, high cut-off frequency, that vacuum transistor demonstrated during simulation makes it attractive for the high-performance analog devices that operates in the THz range. Simulation of the gate-all-around nanowire transistor demonstrated its higher drain current in comparsion to the cathode emission current in the vacuum channel transistor at the same technological nodes. Gate-all-around transistor also showed great ability to the technology scaling, as vertical structure of these transistors could give extremely high placement density.

5. ACKNOWLEDGEMENTS

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