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Scalability analysis of magnetic-nano-junction-based STT-MRAM towards sub-20-nm technology nodes

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ABSTRACT

Here we describe SPICE-compatible compact model of the nano-sized magnetic junction for STT-MRAM at technology nodes beyond 90 nm, where the impact of thermal stability factor and magnetotransport size effects should be taken into account at sub-20 nm dimensions. Within this model it was found that the spatial quantization of the spin-transfer torques which occurs in the magnetic nanobridge based on spin-valve junction (SVJ), when scaling down the nanobridge size below 10 nm, leads to several times higher switching speed, rather than in the case of using magnetic tunnel junctions (MTJ) at the same design rule. Implementation of the current-induced magnetization dynamics into the SPICE model of the nano-sized magnetic junction is based on the equivalent circuit for solving the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation with the effective terms describing the microscopic behavior of spin-transfer torques. This model can be useful for predictive simulation of STT-MRAM performance at advanced technology nodes.

Keywords: STT-MRAM, LLGS, SPICE, MTJ, Spin valve, Magnetic nanobridge, Scalability, Sub-20 nm

INTRODUCTION

Today, an important issue in the development of storage devices is the search for ways to further miniaturize them on the basis of emerging non-volatile memory technologies (FRAM, PRAM, MRAM, RRAM) [1] in order to reduce power consumption and increase the capacity of recorded information compared to existing semiconductor analogues (SRAM, DRAM). One of the promising candidates for the role of RAM and cache memory is STT-MRAM, magnetoresistive memory based on the effect of the transfer of spin angular momentum (spin-transfer torque) between ferromagnetic electrodes in the storage element to change their mutual magnetic configuration and its logical state [2]. The peculiarity of this memory is scalability to technological standards below 22 nm (which is problematic for DRAM [3]), non-volatility, radiation resistance and short cell switching time (comparable to DRAM and SRAM level 3 cache memory [4]). In commercial prototypes of STT-MRAM, the storage element is a magnetic heterostructure consisting of two magnetic layers separated by a thin dielectric layer (MTJ). One layer is assumed to be magnetized in a fixed direction (fixed layer), while the magnetization of the other one (free layer) can be altered by spin-polarized current. Due to the presence of a magnetoresistive effect, the change in the magnetization of the free layer by spin-transfer torque causes a noticeable change in the MTJ resistance, which leads to a change in the logical state in the STT-MRAM cell.

One of the urgent problems in the development of STT-MRAM is the study of the scalability limits of magnetoresistive cell, taking into account the quantization effects arising in the magnetic heterostructure with a decrease in its transverse dimensions to the size of the nanocontact, which is observed at technology nodes below 10 nm [5]. Moreover, below 20 nm, it becomes important to maintain the factor of thermal stability, which depends both on the technology node and on the thickness of the free layer [6]. In this case, during the miniaturization of the cell, changes in the electrophysical parameters of the magnetic structure may occur, affecting the STT-MRAM switching thresholds. In particular, the important task is the consideration of a new form of scalable wire transistors with a round gate (GAA transistor) used both to read and write the STT-MRAM cell state [7] at the minimum design rules (less than 22 nm) that could affect the characteristics of the energy consumption of STT-MRAM.

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In this work, we investigated the scalability of a magnetoresistive memory cell using the BSIM4 predictive technology model for planar transistors with technology nodes scaling from 90 to 22 nm, and examined bulk transistors based on the ballistic FETToy model for FinFET and GAAFET transistors with design rules from 14 to 7 nm and from 7 to 3 nm, respectively [8-10]. It is demonstrated that the reduction of technology node and the quantization of electronic states that occurs when the transverse dimensions of the storage element are reduced to 5 nm will significantly affect the performance of STT-MRAM. The obtained results can be applied in the development of a new generation of scalable memory devices running based on the spin-transfer torque effect.

MODEL AND BASIC EQUATIONS

The STT-MRAM cell consists of an MTJ (which plays the role of a storage cell) and a control transistor (Fig.1).

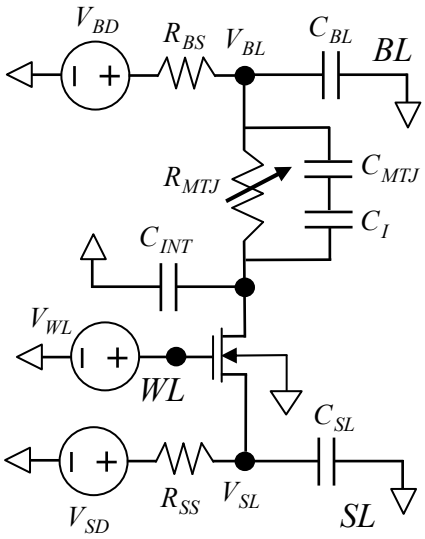

Figure 1. Equivalent circuit of the magnetoresistive cell STT-MRAM (1T-1MTJ) taking into account stray capacitance, where V_{BD} is the bus voltage BD, V_{SD} is the bus voltage SD, V_{WL} is the bus voltage WL, R_{MTJ} is the variable MTJ resistance, R_{BL} is the bus resistance BL, R_{SL} is the bus resistance SL, C_{BL} is the parasitic capacitance of the bus BL, C_{SL} is the parasitic capacitance of the bus SL, C_{INT} is the parasitic capacitance of the bus connection of the MTJ to the drain of the transistor, C_{MTJ} is the capacitance of the dielectric spacer of MTJ, C_I is the capacitance at the interfaces of the MTJ.

Further, because of the small contribution, the stray capacitance of the copper metallization will not be considered.

Magnetic tunnel junction

MTJ is a three-layer structure consisting of two magnetic layers separated by a thin dielectric layer. In this case, the first layer has a fixed magnetization vector (fixed layer), and the second has a free orientation of the magnetization vector (free layer). Depending on the relative position of the magnetization vectors of the two ferromagnetic (FM) layers, the MTJ may be in the antiparallel (when the magnetization vectors are collinear and oppositely directed) and parallel (when the magnetization vectors are collinear and co-directed) state, correspondingly. To change the position of the magnetization vector of the free layer, the effect of transfer of the spin angular momentum from a spin-polarized current is used. This effect is based on the spin transfer from fixed to free FM layer, where the spin-polarized current changes the direction of its magnetization vector.

To describe the physics of the magnetization dynamics of the free layer due to spin-polarized current, the LLGS equation is used:

$$\frac{\partial \vec{m}}{\partial t} = -\gamma_0 \left(\vec{m} \times \vec{H}_{eff}\right) + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} - \frac{\gamma}{M_S d_f}\left(\vec{T}_{\parallel} + \vec{T}_{\perp}\right) \quad (1)$$

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where $\gamma_0 = \mu_0\gamma$, μ_0 is the magnetic constant, γ is the gyromagnetic ratio, α is the phenomenological Gilbert damping coefficient, $\vec{m} = \vec{M}/M_S$ is the unit vector along the magnetization of the free FM layer, d_f is the thickness of the free FM layer, M_S is the saturation magnetization, $\vec{H}_{eff} = \vec{H}_k + \vec{H}_p + \vec{H}$ is the effective magnetic field, which generally includes $\vec{H}$ is the external magnetic field, $\vec{H}_k$ is the in-plane anisotropy field along the unit vector $\vec{e}_Y$, $\vec{H}_p$ is the field perpendicular to the anisotropy direction along the unit vector $\vec{e}_Z$, taking into account the demagnetization field, as well as the field on the interface layers, $\vec{T}_\parallel = T_\parallel(\vec{m} \times \vec{m}_p)$ is the in-plane component of the spin-transfer torque, $\vec{T}_\perp = T_\perp \vec{m}_p$ is the field-like component of the spin-transfer torque, depending on the voltage on the MTJ, $\vec{m}_p$ is the unit magnetization of the fixed FM layer (polarizer), $\vec{m}$ is the unit magnetization of the free FM layer responsible for recording the logical state. To calculate the components of the spin-transfer torques, in our work we used calculations obtained from [11]. To solve the equation (1), we carried out the linearization of the next system of equations:

$$\frac{\partial \vec{m}}{\partial \tau} = -\vec{m} \times \vec{h}_{eff}^{\Sigma} - \alpha \cdot \vec{m} \times \vec{m} \times \vec{h}_{eff}^{\Sigma}, \tag{2}$$

where $\tau = \gamma_0 M_S t/(1+\alpha^2)$ is the dimensionless unit of time, $\vec{h}_{eff}^{\Sigma} = \vec{h}_{eff} + \vec{h}_{STT}^{\parallel} + \vec{h}_{STT}^{\perp}$, $\vec{h}_{eff} = \vec{H}_{eff}/M_S$ is the effective magnetic field, which includes the external magnetic field $\vec{H} = \vec{H}/M_S$, the in-plane anisotropy field $\vec{h}_k = \vec{H}_k/M_S$ and the field of perpendicular anisotropy $\vec{h}_p = \vec{H}_p/M_S$, where $\vec{h}_{STT}^{\parallel} = \tau_\parallel \vec{m} \times \vec{m}_p$, $\vec{h}_{STT}^{\perp} = \tau_\perp \vec{m}_p$, $\tau_{\parallel(\perp)} = \vec{T}_{\parallel(\perp)}(V)/\mu_0 M_S^2 d_f$ is the normalized amplitude of in-plane (perpendicular) spin-transfer torque at given bias voltage V. In this case, equation (2) will be written in projections as:

$$\begin{cases} \frac{dm_X}{d\tau} = \alpha \cdot (m_Y^2 + m_Z^2) h_{effX}^{\Sigma} + (m_Z - \alpha \cdot m_X m_Y) h_{effY}^{\Sigma} - (m_Y + \alpha \cdot m_X m_Z) h_{effZ}^{\Sigma} \\ \frac{dm_Y}{d\tau} = -(m_Z + \alpha \cdot m_X m_Y) h_{effX}^{\Sigma} + \alpha \cdot (m_X^2 + m_Z^2) h_{effY}^{\Sigma} + (m_X - \alpha \cdot m_Y m_Z) h_{effZ}^{\Sigma} \\ \frac{dm_Z}{d\tau} = (m_Y - \alpha \cdot m_X m_Z) h_{effX}^{\Sigma} - (m_X + \alpha \cdot m_Y m_Z) h_{effY}^{\Sigma} + \alpha \cdot (m_X^2 + m_Y^2) h_{effZ}^{\Sigma} \end{cases}, \tag{3}$$

Next, we will solve equation (3) by numerical methods, such as the Runge-Kutta method. By analogy with the Runge-Kutta method [12], we will do a circuit implementation of the LLGS equation, where the physical parameters are replaced by the electrical parameters of the equivalent circuit: capacitance $C = (1+\alpha^2)/\gamma_0 M_S$, voltage $V_\mu = m_\mu$ and alternating current i_μ, the components of which are described in the form of the following equations:

$$\begin{cases} i_X = \alpha \cdot (V_Y^2 + V_Z^2) h_{effX}^{\Sigma} + (V_Z - \alpha \cdot V_X V_Y) h_{effY}^{\Sigma} - (V_Y + \alpha \cdot V_X V_Z) h_{effZ}^{\Sigma} \\ i_Y = -(V_Z + \alpha \cdot V_X V_Y) h_{effX}^{\Sigma} + \alpha \cdot (V_X^2 + V_Z^2) h_{effY}^{\Sigma} + (V_X - \alpha \cdot V_Y V_Z) h_{effZ}^{\Sigma} \\ i_Z = (V_Y - \alpha \cdot V_X V_Z) h_{effX}^{\Sigma} - (V_X + \alpha \cdot V_Y V_Z) h_{effY}^{\Sigma} + \alpha \cdot (V_X^2 + V_Y^2) h_{effZ}^{\Sigma} \end{cases}, \tag{4}$$

where $\mu = x, y, z$, as a result of which the LLGS equations (4) can be represented as a system of coupled dynamic equations $i_\mu = C\frac{dV_\mu}{dt}$, which is illustrated in Fig. 2.

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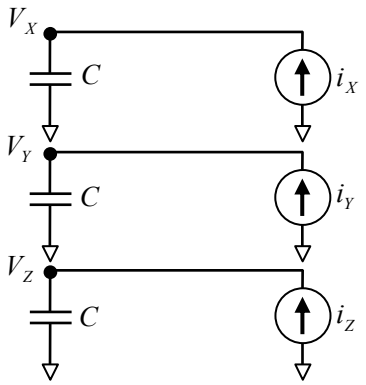

Figure 2. The equivalent circuit for the integration of the LLGS equation in HSPICE model of the magnetoresistive memory cell of STT-MRAM.

The specified position of the magnetization of the free FM layer corresponds to a certain value of the MTJ resistance, which is described by the equation:

$$R_{MTJ} = 2\frac{V_{MTJ}}{S_{MTJ}\cdot\left(J^{P}_{MTJ}\left(1+m_Z\right)+J^{AP}_{MTJ}\left(1-m_Z\right)\right)} \tag{5}$$

where V_{MTJ} is the bias voltage applied on MTJ, S_{MTJ} is the cross-sectional area of MTJ, $J^{P(AP)}_{MTJ} = J^{P(AP)}_{MTJ}(V_{MTJ})$ is the dependence of the current density on the voltage V_{MTJ} on the tunnel structure for the P (AP) state of magnetization of the free FM layer. In turn, the dependence $J^{P(AP)}_{MTJ} = J^{P(AP)}_{MTJ}(V_{MTJ})$ can be obtained from direct quantum mechanical calculations of the tunneling characteristics of MTJ and the voltage $V_{MTJ} = V_{IN} - V_{OUT}$ is considered as the difference between the voltage of the electrical node at the input (V_{IN}) and the voltage of the electrical node at the output (V_{OUT}) of MTJ. This approach allows to use the MTJ model in SPICE environments, which, in turn, gives the possibility to accelerate the development of schemes using STT-MRAM cells.

Control transistor

To control the spin-polarized current, it is necessary to use a control transistor. This transistor allows you to switch the STT-MRAM cell in different modes: read or write mode. Currently, there are a huge number of different types of field-effect transistors and their models. In addition to the planar transistor, widely used in industry and described within the Berkeley BSIM4 model, with the development of high-performance and high-density integrated circuits for personal computers a great interest in new types of field-effect transistors (FET) is increasing: double gate (or tri-gate) FinFET and their improvement for lower technology nodes - GAA (gate-all-around) FET (Figure 3, 4).

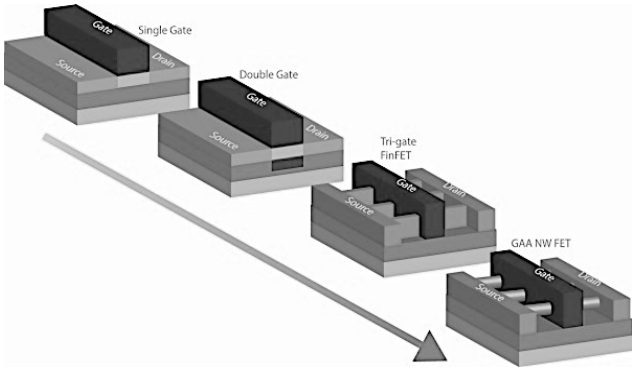

Figure 3. The evolution of the transistor from planar MOSFET to bulk GAA FET.

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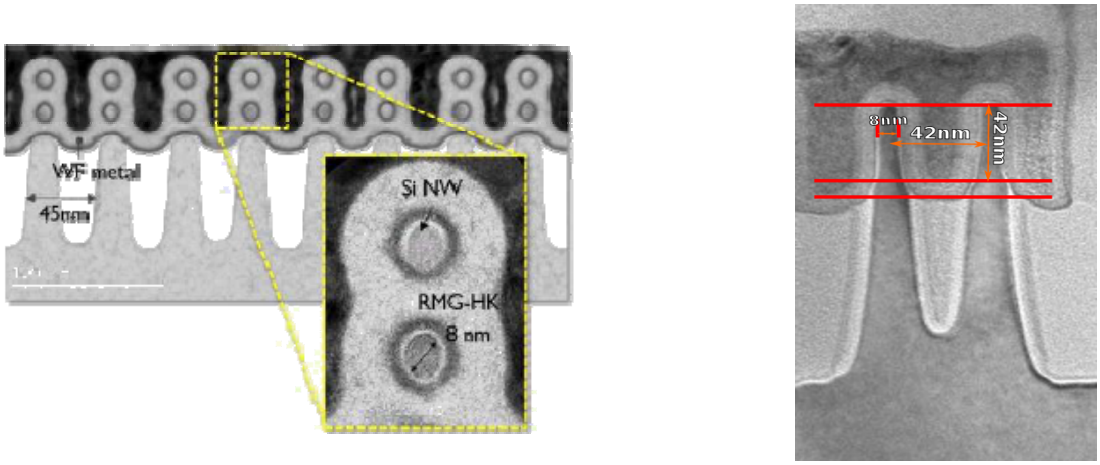

(a) (b)

Figure 4. (a) NW GAA FET from Imec with the topology of 8 nm (2016) and (b) FinFET from Intel with a topology of 14 nm [13, 14].

To simulate the control transistors (FinFET and GAA FET) with a predetermined design rule, a compact FET-Toy model (developed by Purdue University, Florida, Illinois in Urbana-Champaign, Southern Illinois in Carbondale and IBM) was used [10]. To model planar FET transistors at technology nodes from 90 to 22 nm, the parameters taken from the BSIM4 predictive technology FET model were used [10]. The parameters of FinFET and GAA FET transistors are taken from the Wikichip website [14] and are presented in the Table 1. Table 2 shows the signal order for reading and writing state in a magnetoresistive memory cell of STT-MRAM.

Table 1. Geometric parameters of FinFET and GAA FET for SPICE simulation.

	FinFET			**GAA NW FET**		
Topology node (nm)	14	10	7	7	5	3
EOT (nm)	0.9	0.8	0.7	0.65	0.6	0.55
Hfin (nm)	35	40	45	-	-	-
Wfin (nm)	8	7	6	-	-	-
Diameter (nm)	-	-	-	7	5	3

Table 2. Signal table for read/write magnetic state in «1T-1MTJ» STT-MRAM cell (Figure 1), where V_R – read voltage, V_{WR} – write voltage, V_{DD} – supply voltage.

Line	**Read P/AP**	**Write P/AP**
BL	$V_{BD}=V_R$	$V_{BD}=V_{WR}/0$
SL	$V_{SD}=0$	$V_{SD}=0/V_{WR}$
WL	$V_{WL}=V_{DD}$	$V_{WL}=V_{DD}=V_{WR}$

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Spin-valve magnetic nano-bridge structure

To further improve the performance of STT-MRAM at nodes below 7 nm, in our work we have studied the effect of quantization of the spin-transfer torques in the magnetic nanobridge Au/Co/Au/Co/Au (Figure 5).

Conductance quantization at a room temperature was firstly observed in metal nonmagnetic contacts Au/Au, Cu/Cu, Pt/Pt [15-17]. One of the very promising structure is a nanoscale spin valve consisting of Co/Au/Co trilayer [18-20]. This is due to the possibility of technological reduction of the diameter of Au nanowires to 0.6 nm, which was shown in [18]. In addition, [19] demonstrated a sufficiently high value of magnetoresistance in such a nanocontact–about 73%. In the magnetic nanobridge containing two ferromagnetic layers separated by a tunnel or metallic nonmagnetic spacer, not only the magnetoresistance but also the spin-transfer torque is quantized. This can additionally affect the spin dynamics in such nanostructures. Therefore, the quantized components of spin-transfer torques from [21] were used to study the characteristics of STT-MRAM based on magnetic nanobridge at technology nodes below 7 nm.

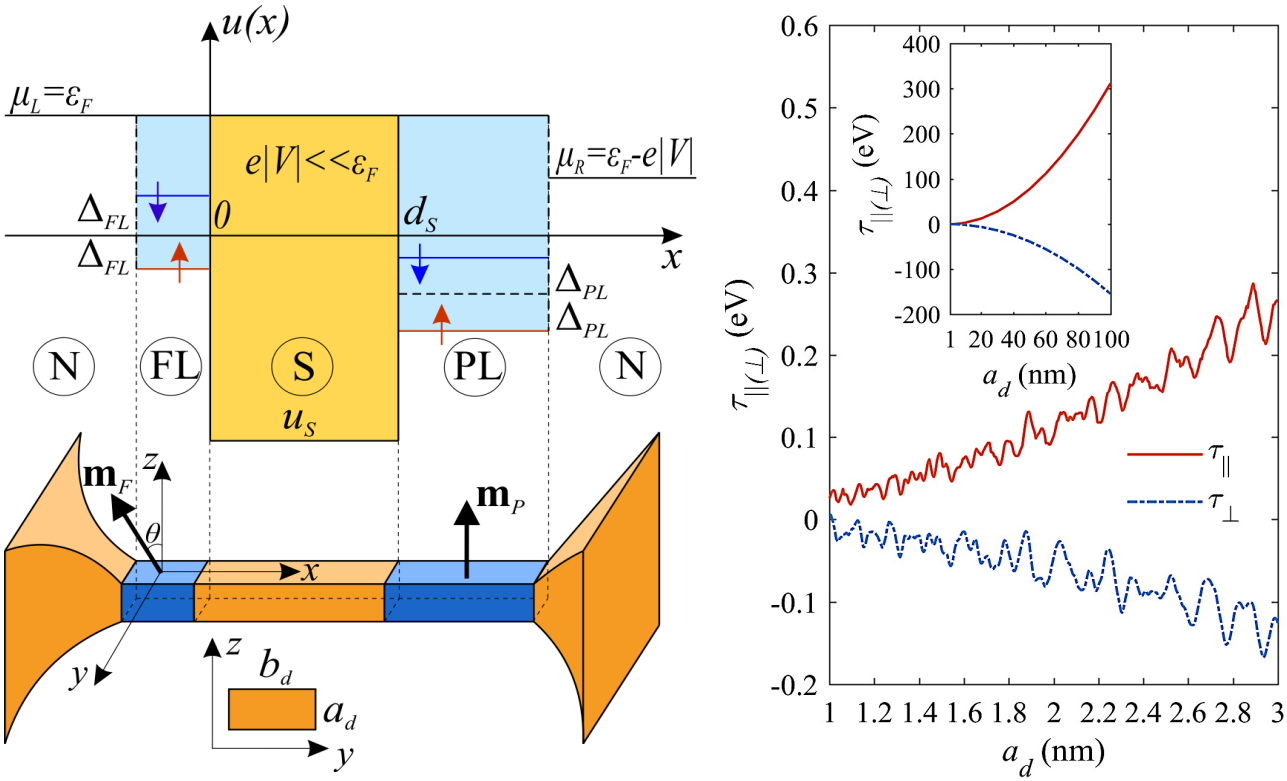

Figure 5. (a) Schematic of the potential energy $u(x)$ of conduction electrons in the nanobridge with the FL/S/PL spin valve connected to bulk metallic N contacts, where PL (FL) is the fixed (free) magnetic layer and S is the metallic spacer (in the low voltage approximation, when $e|U| \ll \varepsilon_F$). The lower inset shows the rectangular cross section of the bridge with the thickness a_d and the width b_d. The vector $\boldsymbol{m_p}$ is equivalent to $\boldsymbol{m_p} = (1,0,0)$ and $\boldsymbol{e_x}, \boldsymbol{e_y}, \boldsymbol{e_z}$ are the unit vectors of the Cartesian coordinate system. (b) Amplitudes of the in-plane $\tau_\parallel$ and perpendicular $\tau_\perp$ components of the spin-transfer torque in the Au/Co/Au/Co/Au magnetic bridge versus the thickness a_d of its rectangular cross section with the aspect ratio $b_d/a_d = 2$ at the bias voltage $U = 0.1$ V. The inset shows the amplitudes $\tau_\parallel$ and $\tau_\perp$ versus a_d varied in the range up to 100 nm.

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Thermal stability factor

An important criterion ensuring the extended scalability of nonvolatile magnetoresistive memory (STT-MRAM), based on spin-transfer-torque phenomena in MTJs, towards sub-20-nm technology node is the possibility to maintain high thermal stability (>80k_BT) when demonstrating low switching voltage (not more than 0.5 V) at reduced MTJ dimensions. It was found in [6, 22], that at such technology nodes a good thermal stability can be achieved by increasing the magnetic anisotropy field with the thickness of free layer.

The energy E_b required to switch the memory between these two states at temperature T is characterized by the dimensionless thermal stability factor Δ_T. In macrospin approximation, this factor is given by the next equation:

$$\Delta_T = \frac{E_b}{kT} = \frac{\pi D^2}{4k_B T}\left(\frac{1}{2}\mu_0(N_{xx} - N_{zz}) + K_i + K_B t\right) \quad (6)$$

where D is the diameter of the MTJ, k_B is the Boltzmann constant, μ_0 is the vacuum magnetic permeability, K_i is the interfacial anisotropy at the dielectric/ferromagnetic interface, K_B is the bulk anisotropy, t is the thickness of the free FM layer, N_{xx} and N_{zz} are the in-plane and out-of-plane demagnetizing factors respectively.

For the standard CoFeB/MgO/CoFeB in-plane MTJs, $N_{xx} - N_{zz}$=-1 (with a free layer thickness of 1.4 nm, which is significantly smaller than the diameter (>20 nm) of the MTJ) leads to a negative shape anisotropy, which plays the role of the MTJ demagnetization field. On the contrary, the strong positive interfacial anisotropy K_i acts against the demagnetizing anisotropy. The contribution of the bulk anisotropy K_B to the magnetization of the material is extremely small and is usually neglected in the conventional in-plane MTJ.

However, with an increase in the thickness of the free layer, the expression, $N_{xx} - N_{zz} = 1 - \frac{1}{1+\frac{4t}{D\sqrt{\pi}}} = 1 - 2N_{xx}$ becomes positive and this leads to a positive anisotropy shape, which pulls the magnetization vector of the free layer out of the plane. This effect was described in more detail in articles [20, 21]. In this work the calculations of the thermal stability factor were carried out, depending on the thickness of the free layer and diameter of the MTJ.

RESULTS

As a result of the circuit simulation of the STT-MRAM cell, the temporal characteristics of the current and resistance for various design standards were obtained. To calculate the averaged write current, consumed energy and recording power, we used the next equations:

$$\langle I_{WR} \rangle = \frac{1}{\tau}\int_0^{\tau} I_W(t)dt \quad (7)$$

$$E_{WR} = \int_0^{\tau} |V_{BL} - V_{SL}| I_W(t)dt \quad (8)$$

$$P_{WR} = E_{WR}/\tau \quad (9)$$

where τ is the write time. The obtained values of these parameters for different technology nodes are presented in the Table 3-6 below.

Table 3. Averaged current, power, energy and time for switching the magnetoresistive cell of STT-MRAM with a planar control transistor from P to AP state, and vise versa, at technology nodes varied from 90 to 22 nm.

Technology node, nm	**90**	**65**	**45**	**32**	**22**
Avg. current $\langle I_{WR} \rangle^{P\to AP}$, µA	127.6	38.632	22.678	12.488	7.0884
Avg. current $\langle I_{WR} \rangle^{AP\to P}$, µA	278.72	123.38	74.904	43.04	17.674
The switching time. $\tau^{P\to AP}$, ns	6	6	6	6	6

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The switching time. $\tau^{AP\to P}$, ns	1	1	1	1	1
Power $P^{P\to AP}$, µW	153.12	42.495	22.678	11.239	5.6707
Power $P^{AP\to P}$, µW	334.47	135.72	74.904	39.153	14.139
Energy $E^{P\to AP}$, pJ	0.9187	0.25497	0.13607	0.10115	0.051036
Energy $E^{AP\to P}$, pJ	0.33447	0.12201	0.074904	0.0587	0.014139
Voltage supply, V	1.2	1.1	1	0.9	0.8

Table 4. Averaged current, power, energy and time for switching the magnetoresistive cell of STT-MRAM with a FinFET control transistor from P to AP state, and vise versa, at technology nodes varied from 14 to 7 nm.

Technology node, nm	**14**	**10**	**7**
Avg. current $\langle I_{WR}\rangle^{P\to AP}$, µA	6.8484	2.5917	1.0262
Avg. current $\langle I_{WR}\rangle^{AP\to P}$, µA	6.5844	2.5754	1.0155
The switching time. $\tau^{P\to AP}$, ns	5	5	5
The switching time. $\tau^{AP\to P}$, ns	0.9	1.3	1.8
Power $P^{P\to AP}$, µW	4.4514	1.2958	0.41047
Power $P^{AP\to P}$, µW	4.2798	1.2877	0.40622
Energy $E^{P\to AP}$, fJ	0.022257	0.0064792	0.0020523
Energy $E^{AP\to P}$, fJ	0.0038518	0.0016740	0.00073119
Voltage supply, V	0.65	0.5	0.4

Table 5. Averaged current, power, energy and time for switching the magnetoresistive cell of STT-MRAM with a GAA FET control transistor from P to AP state, and vise versa, at technology nodes varied from 7 to 3 nm.

Technology node, nm	**7**	**5**	**3**
Avg. current $\langle I_{WR}\rangle^{P\to AP}$, µA	1.0012	0.47777	0.16476
Avg. current $\langle I_{WR}\rangle^{AP\to P}$, µA	0.97666	0.45460	0.15560
The switching ti\me. $\tau^{P\to AP}$, ns	4.8	4.9	5
The switching time. $\tau^{AP\to P}$, ns	1.9	2	2.1
Power $P^{P\to AP}$, µW	0.40047	0.17677	0.057666
Power $P^{AP\to P}$, µW	0.39066	0.16820	0.054460
Energy $E^{P\to AP}$, fJ	0.0019222	0.00086619	0.00029
Energy $E^{AP\to P}$, fJ	0.00074	0.00033	0.00011
Voltage supply, V	0.4	0.37	0.35

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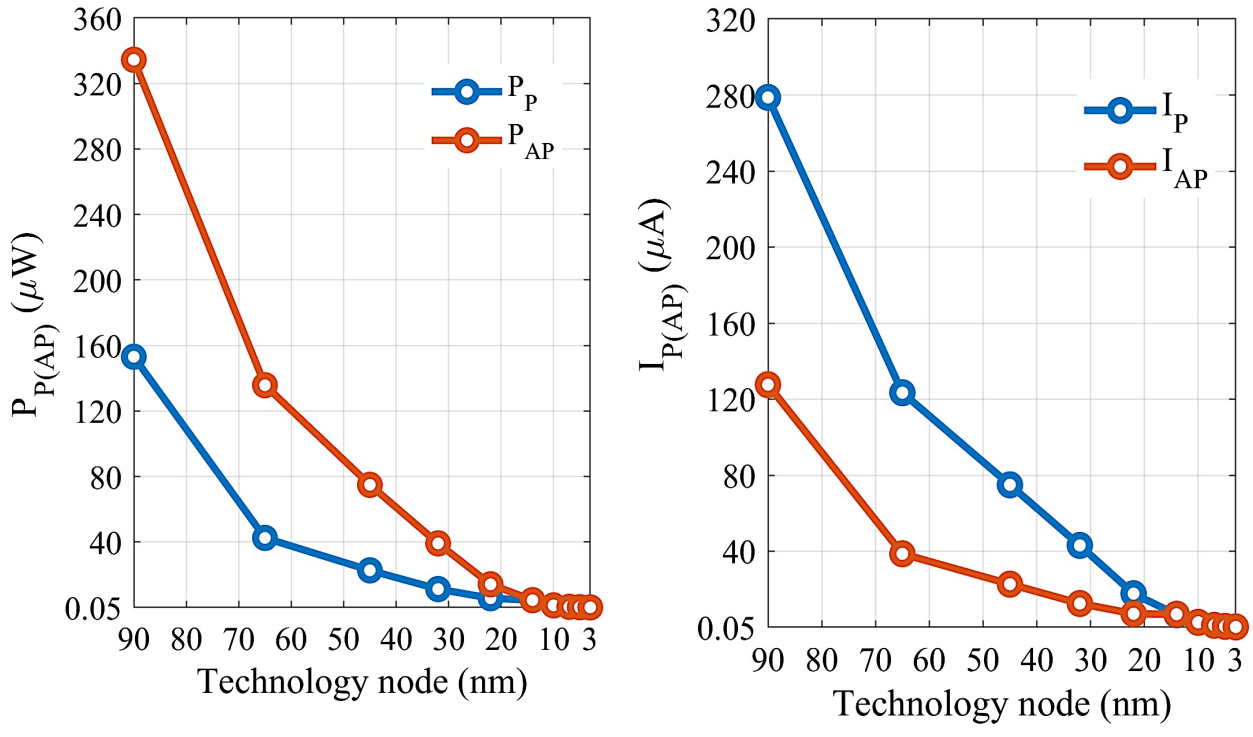
Table 6. Averaged current, power, energy and time for switching the magnetoresistive STT-MRAM cell based on an Au / Co / Au / Co / Au magnetic bridge with a GAA FET control transistor from P to AP state, and vise versa, at technology nodes varied from 7 to 3 nm.

Technology node, nm	**7**	**5**	**3**
Avg. current $\langle I_{WR}\rangle^{P\to AP}$, μA	5.0263	2.6879	1.8464
Avg. current $\langle I_{WR}\rangle^{P\to AP}$, μA	5.0262	2.6879	1.8463
The switching time. $\tau^{P\to AP}$, ns	1.4	1.4	0.8
The switching time. $\tau^{AP\to P}$, ns	1.7	1.5	1.4
Power $P^{P\to PA}$, μW	2.0105	0.99453	0.64624
Power $P^{AP\to P}$, μW	2.0105	0.99451	0.64621
Energy $E^{P\to AP}$, fJ	0.0028147	0.0013923	0.00051699
Energy $E^{AP\to P}$, fJ	0.0034178	0.0014918	0.0009047
Voltage supply, V	0.4	0.37	0.35

A summary of the calculation of power consumption and averaged current depending from the technology node of the MTJ is shown below in Figure 6.



(a) (b)

Figure 6. (a) Power consumption and (b) averaged current for switching the magnetoresistive cell of STT-MRAM from P (AP) to AP (P) state, depending from the technology node.

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From the above graphs, it can be easily seen that with scaling down the technology node for STT-MRAM from 90 to 3 nm, the power consumption decreased by almost 6200 times in the case of switching the cell from anti-parallel to parallel state and 2700 times in the opposite case. Also, the switching time of the STT-MRAM cell decreased from 6 ns (at 90 nm) to 5 ns (3 nm) and increased from 1 ns (at 90 nm) to 2.1 ns (3 nm) for switching cells from parallel to anti-parallel and back respectively.

Interesting results were obtained in the case of quantization of the spin-transfer torque components in magnetic nanowires. So, in comparison with conventional MTJ with the same design standards, a magnetic nanowire shows almost 6 times higher switching speed from a parallel state to an antiparallel one (5 ns for MTJ and 0.8 ns for nanowire at technology node of 3 nm, respectively).

However, with the transition to the node below 7 nm with the GAA FET control, the drain current drops sharply, for a stable switching of the STT-MRAM cell it is necessary to maintain a supply voltage of about 0.4-0.35 V. Otherwise, the switching time of the state increases or memory cell does not switch. The switching graphs of the current for the MTJ and for the magnetic nanowire are shown correspondingly in Figure 7.

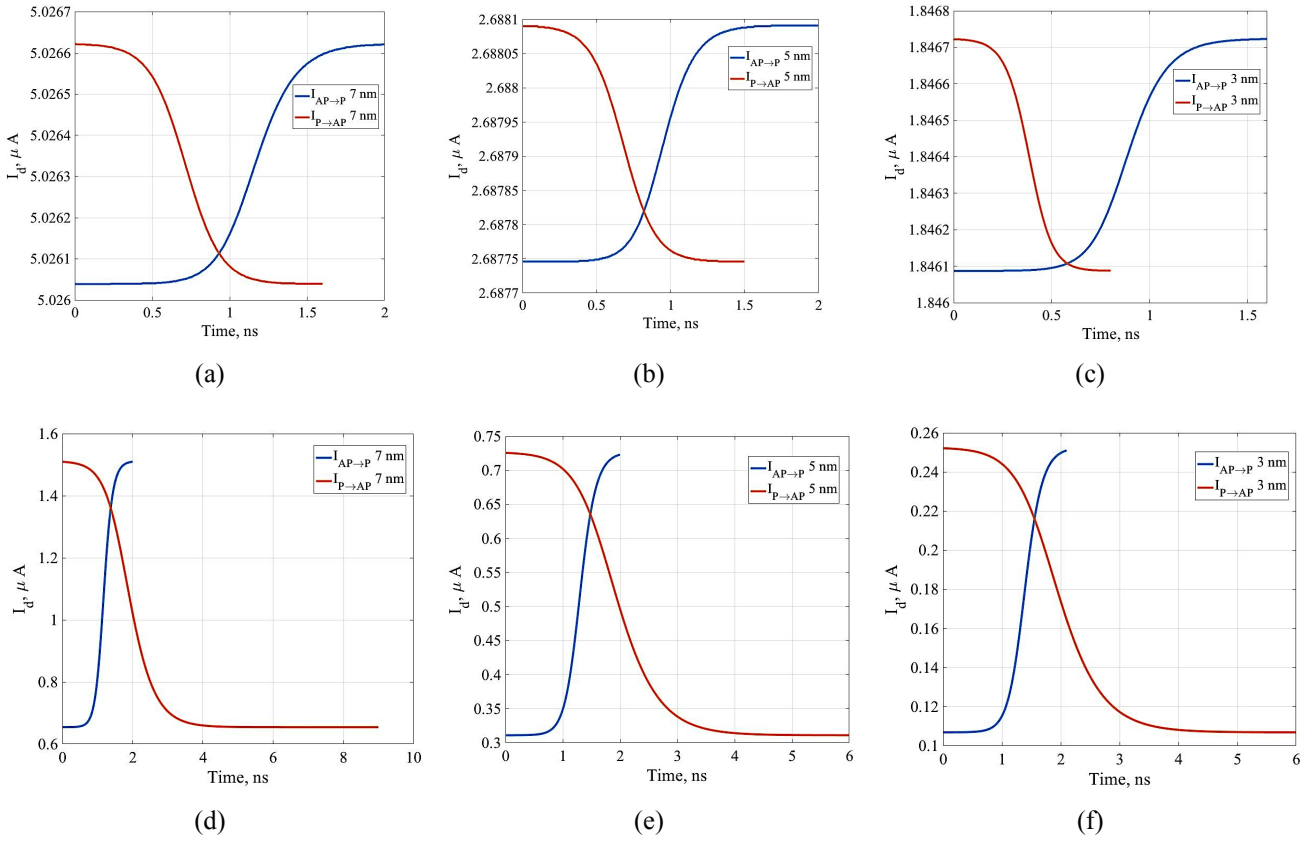

Figure 7. Switching characteristics of the current when switching the STT-MRAM cell for various technology nodes: for the magnetic nanobridge (a-c) and for the MTJ (d-f)

Also, in our work, the factor of thermal stability was calculated, depending on the thickness of the FL and the diameter of MTJ. Thus, using equation (6) and the values of the MTJ parameters from article [6], the diagram of thermal stability factor presented below in Figure 8 was obtained.

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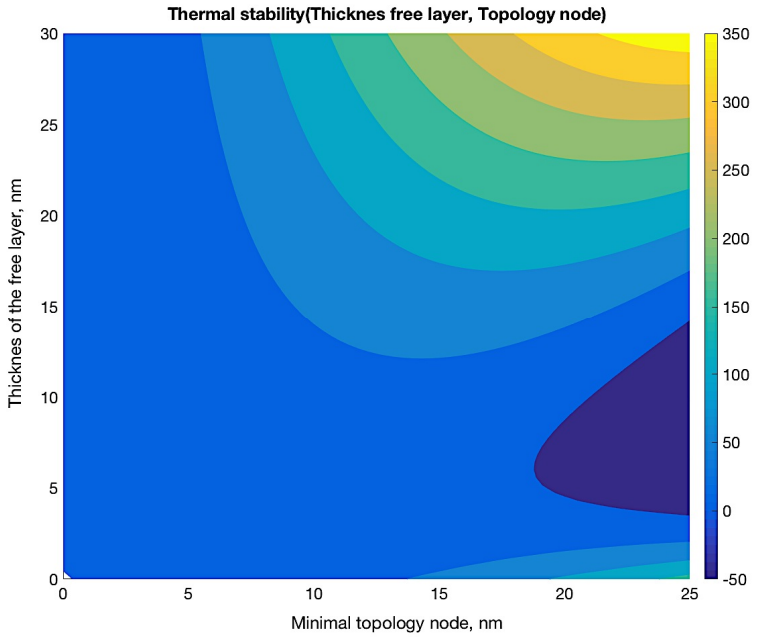

Figure 8. The diagram of thermal stability of MTJ depending on the thickness of the free layer and minimal topology node equal to the diameter of MTJ.

From the thermal stability diagram, it was found that with an increase in the thickness of the FL of MTJ, the factor of thermal stability increases and, at technology nodes of about 20-25 nm, when the thickness of the free layer is varied from 5 to 15 nm, the free layer of MTJ changes its magnetization direction from the out-of-plane to the in-plane one. Also, as you can see from the graph, at design rules of about 5 nm, the free layer thickness should be 27–30 nm to obtain a thermal stability factor of about 60.

CONCLUSION

The result of this work was the circuit design of the magnetoresistive cell of STT-MRAM for technology nodes varied from 90 to 3 nm using planar MOSFET, volume FinFET and GAA FET control transistors. For dimensions below 10 nm (7, 5, 3 nm), the structure of the type Au/Co/Au/Co/Au was also proposed as a storage element of STT-MRAM with the effect of quantized spin-transfer torques. It was shown that the scaling of STT-MRAM leads to a significant reduction in energy consumption (more than 6000 times, from ~ 330 μW at 90 nm to ~ 0.05 μW at 3 nm). It was also shown that the switching time of the STT-MRAM cell can be reduced by using the Au/Co/Au/Co/Au structure, which is more than 6 times faster than the CoFe/MgO/CoFe structure.

To solve the problem of reducing thermal stability at technology nodes below 20 nm, the contribution of shape-anisotropy with increasing thickness of the free layer of MTJ was considered, as it is shown in Figure 8.

This model showed an increase in the thermal stability factor with an increase in the thickness of the free layer of the MTJ, which made it possible to obtain a thermal stability factor of about 60 with technology node of 5 nm and the free layer thickness of about 27 nm. These results can be useful for further research and development of sub-20-nm STT-MRAM.

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